بسم الله الرحمن الرحيم

السلام عليكم ورحمة الله وبركاته

Graphene Nanoribbon Modelling CMOS

Written by
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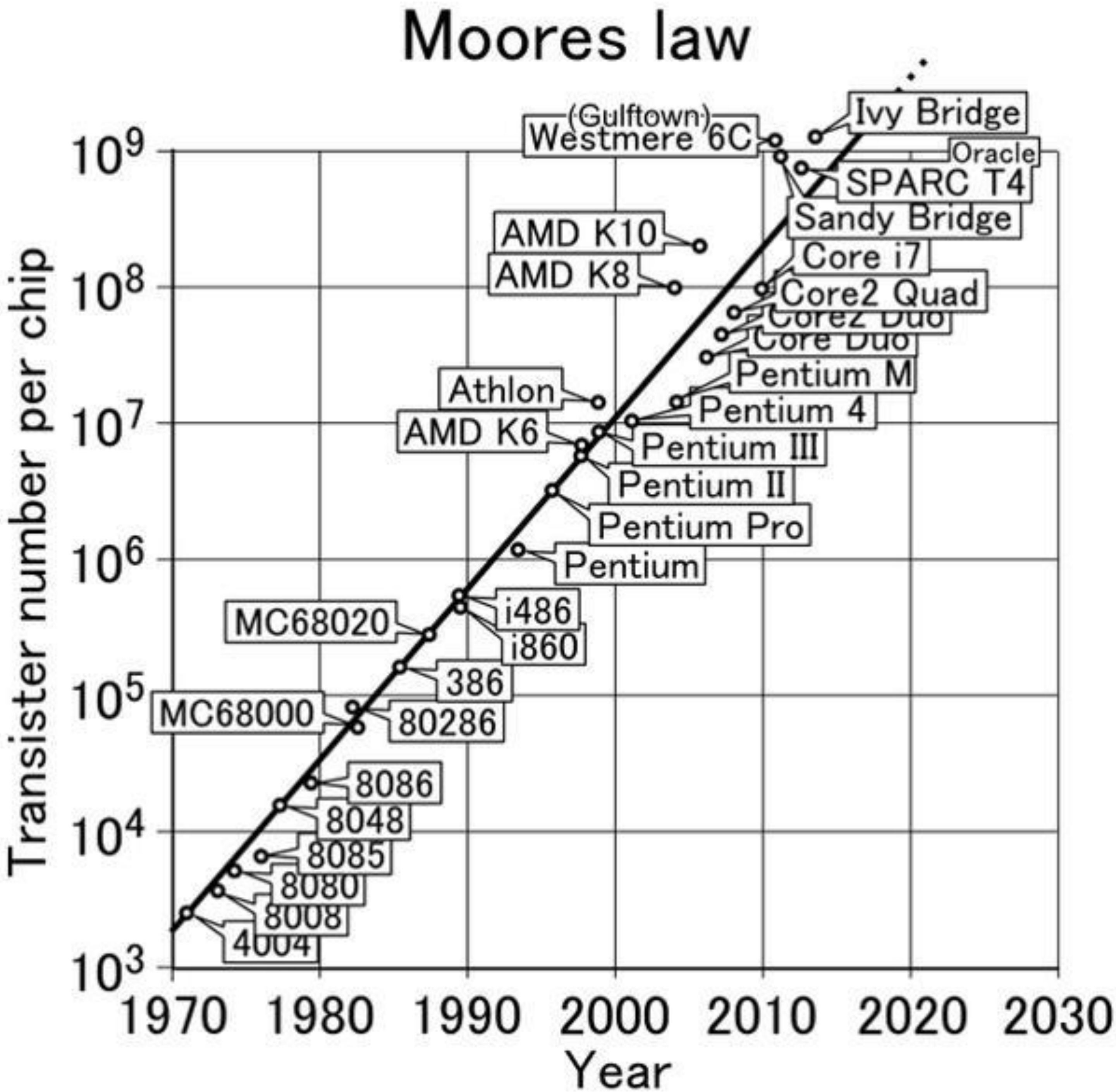
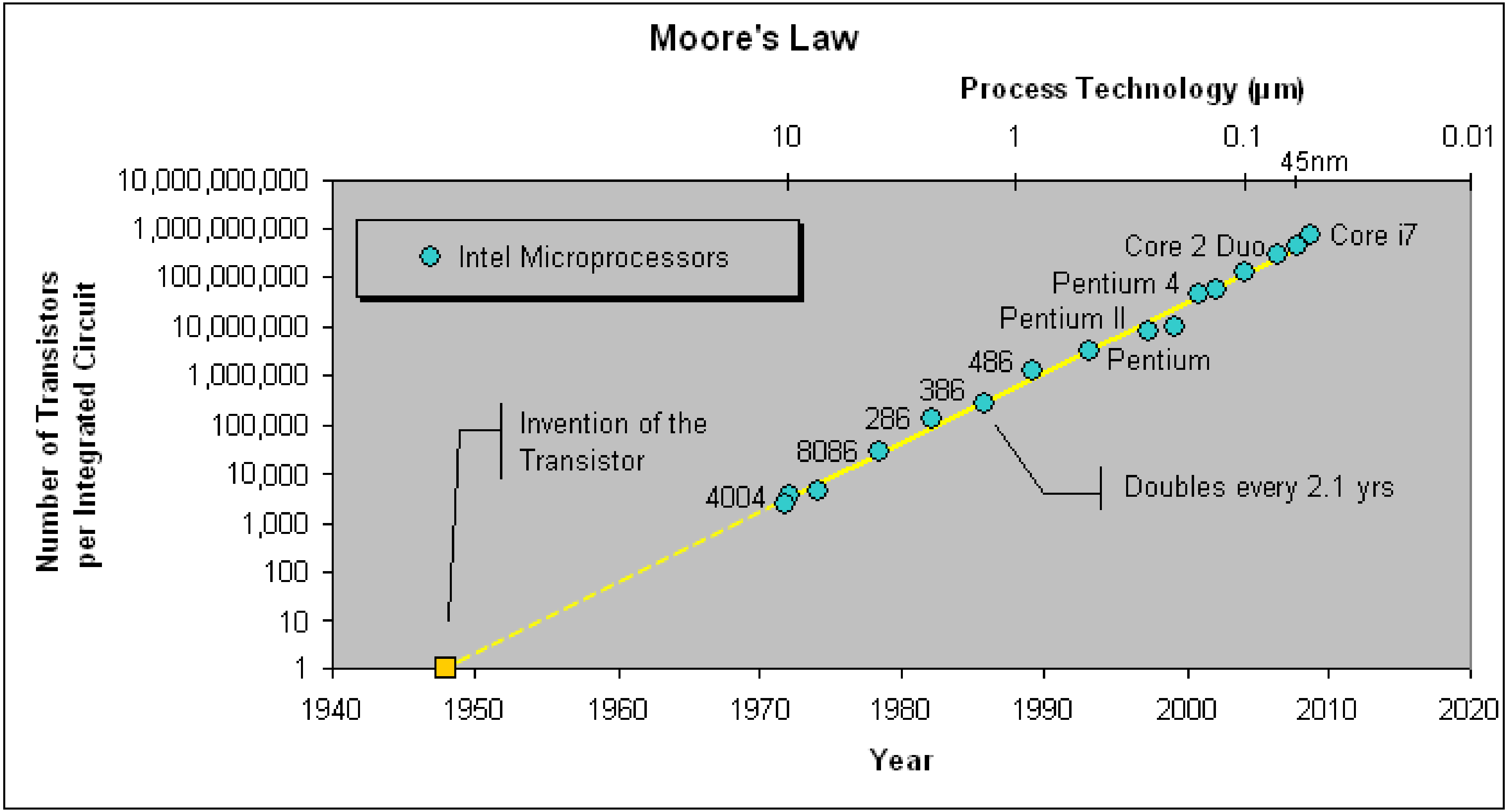
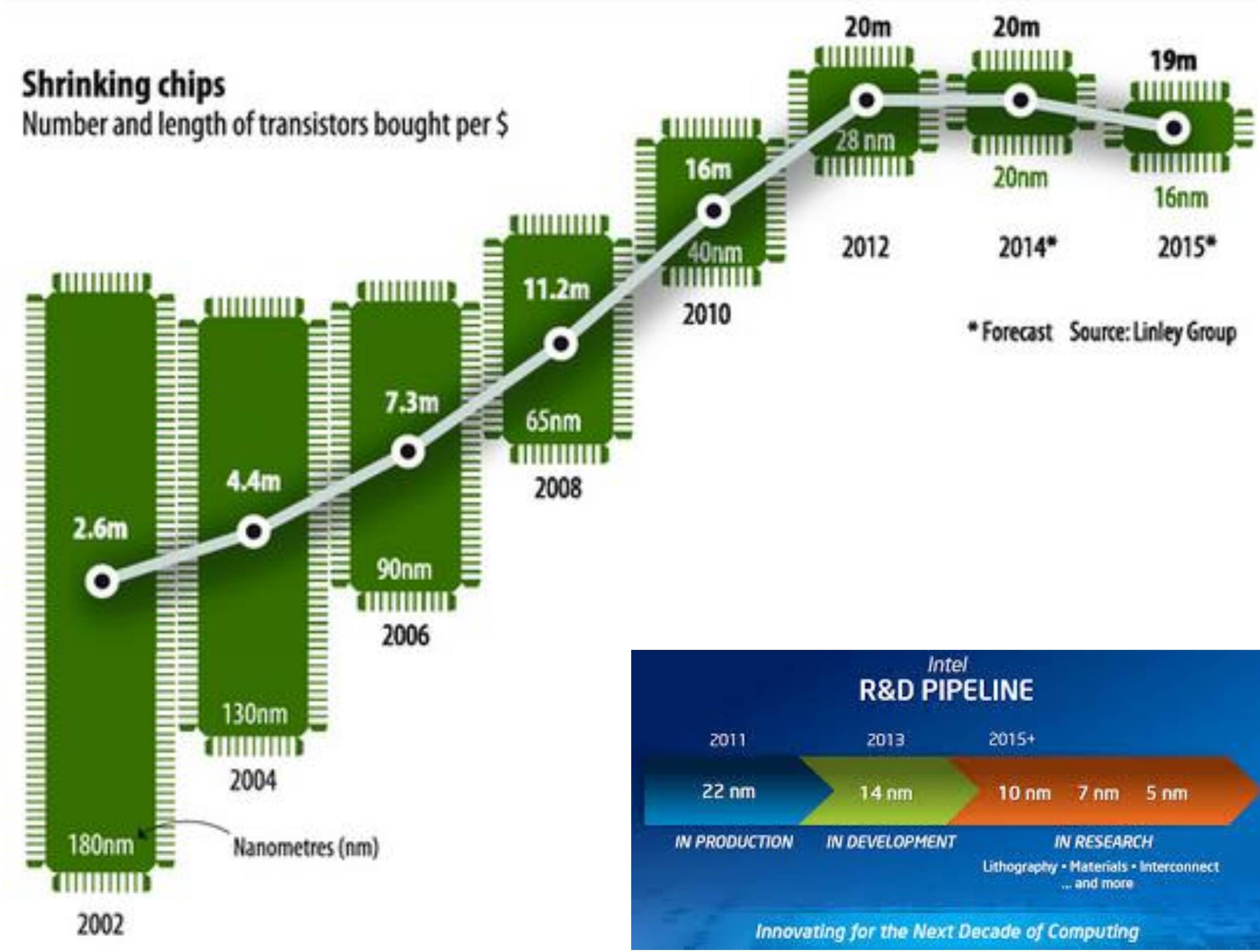


Moores law
Transister number per chip
Year
10^9
10^8
10^7
10^6
10^5
10^4
10^3
1970
1980
1990
2000
2010
2020
2030
4004
8008
8080
8085
8048
8086
MC68000
80286
386
MC68020
i486
i860
Pentium
Pentium Pro
Pentium II
Pentium III
AMD K6
Athlon
Pentium 4
Pentium M
Core Duo
Core2 Duo
Core2 Quad
Core i7
AMD K8
AMD K10
Sandy Bridge
Oracle
SPARC T4
(Gulftown)
Westmere 6C
Ivy Bridge


Moore's Law
Process Technology (µm)
10
1
0.1
0.01
45nm
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
100
10
1
Number of Transistors per Integrated Circuit
Intel Microprocessors
Core i7
Core 2 Duo
Pentium 4
Pentium II
Pentium
486
386
286
8086
4004
Invention of the Transistor
Doubles every 2.1 yrs
1940
1950
1960
1970
1980
1990
2000
2010
2020
Year

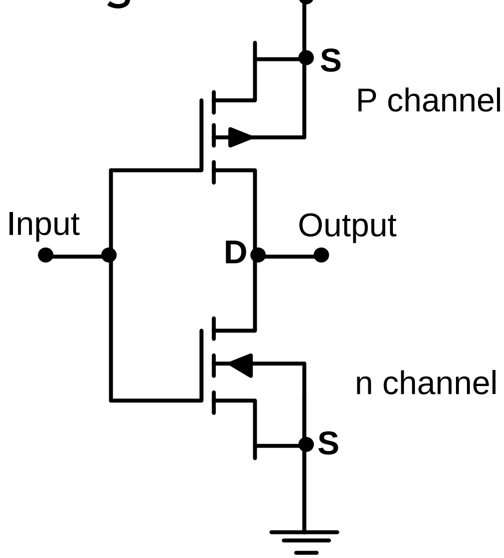

Shrinking chips
Number and length of transistors bought per $
2.6m
180nm
2002
4.4m
130nm
2004
7.3m
90nm
2006
11.2m
65nm
2008
16m
40nm
2010
20m
28 nm
2012
20m
20nm
2014*
19m
16nm
2015*
Nanometres (nm)
* Forecast Source: Linley Group
Intel
R&D PIPELINE
2011
2013
2015+
22 nm
14 nm
10 nm
7 nm
5 nm
IN PRODUCTION
IN DEVELOPMENT
IN RESEARCH
Lithography • Materials • Interconnect
... and more
Innovating for the Next Decade of Computing

CMOS

- Most commonly, stands for Complementary Metal Oxide Semiconductor, is a low-power, low-heat semiconductor technology ,it is used to refer to small battery-powered configuration chips on system boards of personal computers.
- The continuous scaling of transistors in the last half of century has been the driving force for electronics. The channel length of the transistors in production today is below 100nm. A wide variety of devices are also being explored to complement or even replace silicon transistors at molecular scales.

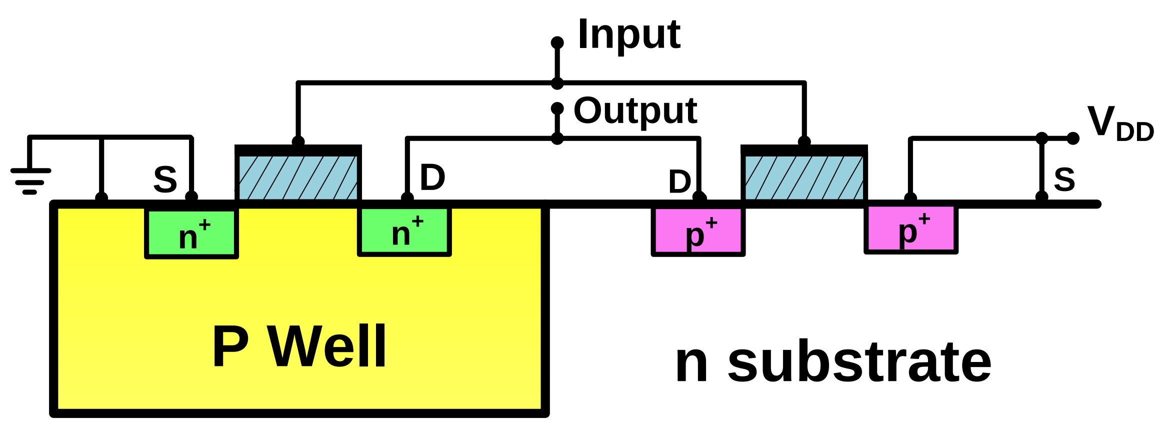
CMOS

- The p-well process has been a commonly used technique for CMOS.
- The p-type substrate doping level larger than the n-type substrate doping level to obtain the desired VT.
- the n-well doping controlled by ion implantation.
- The twin well CMOS process are allows both the p-well and n-well regions.



CMOS inverter circuit

$$V_{GS}=V_G-V_S$$
$$V_{DS}=V_D-V_S$$



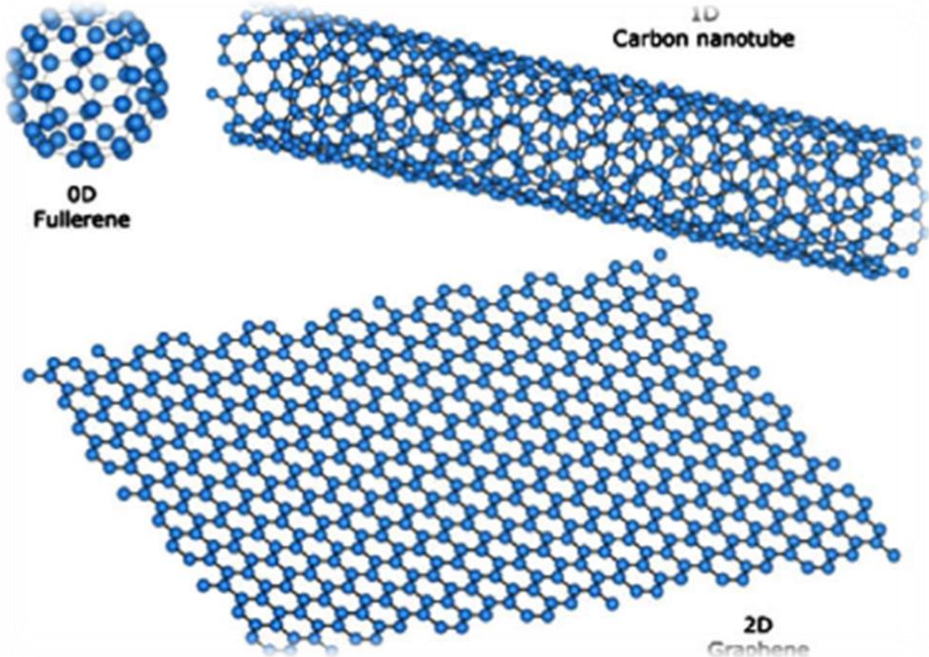
Simplified IC cross-section of CMOS inverter

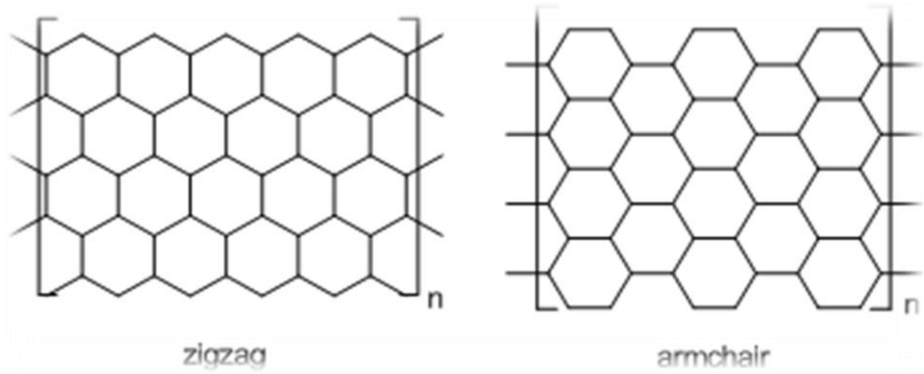
graphene nanoribbon (GNR)

- Graphene as a Single and few layers of carbon sheets, have been fabricated by different kinds of techniques including mechanical exfoliation and chemical vapor deposition (CVD).
- The unique band structure, transport properties, and thermodynamic stability make it a very promising material for high-frequency FET and beyond complementary metal–oxide–semiconductor (CMOS) nano-electronic devices
- Graphene has attracted attention as a high-mobility channel replacement for Si in MOSFETs for high frequency applications.

GRAPHENE NANORIBBON (GNR)

Low-dimensional carbon allotropes: fullerene (0D), carbon nanotube (1D) and graphene (2D).

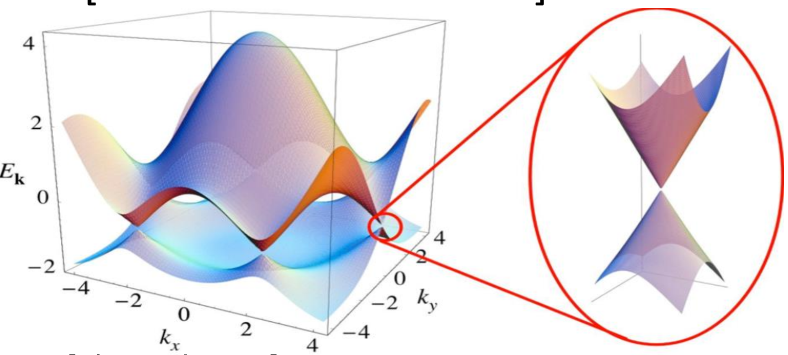




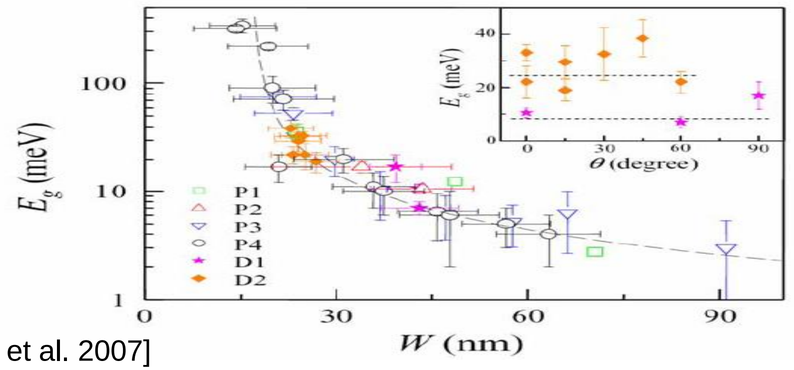
Graphene nanoribbons possess semiconductive properties and may be a technological alternative to silicon semiconductors.

- Tight binding calculations show that armchair type can be semiconducting or metallic depending on width.
- Zigzag edges provide the edge localized state with non-bonding molecular orbital’s near the Fermi energy.
- Tight binding calculations show that zigzag type is always metallic.

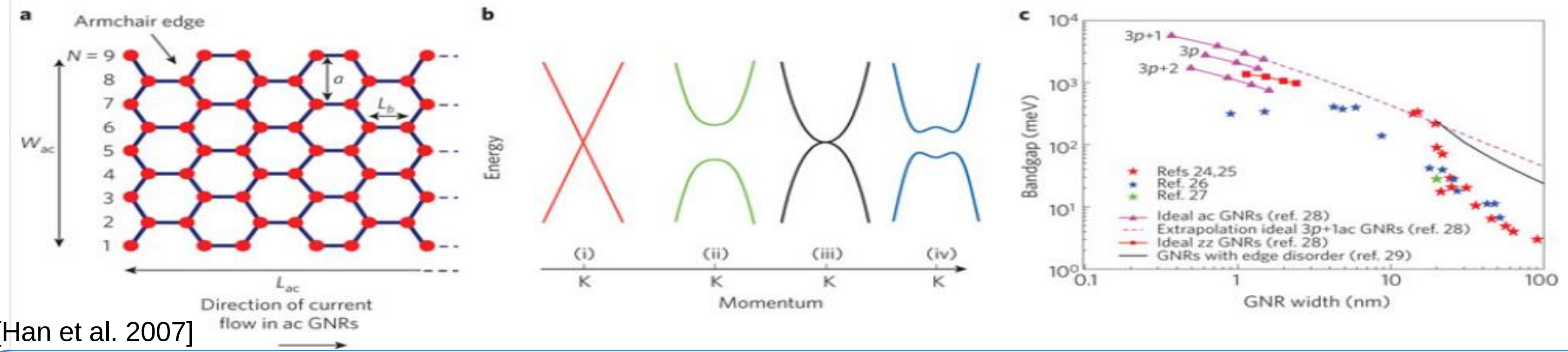
Graphene is a gapless material with charge carriers behaving as massless Dirac Fermions [Castro Neto et.al 2009]



[Kim et al. 2006]



[Han et al. 2007]

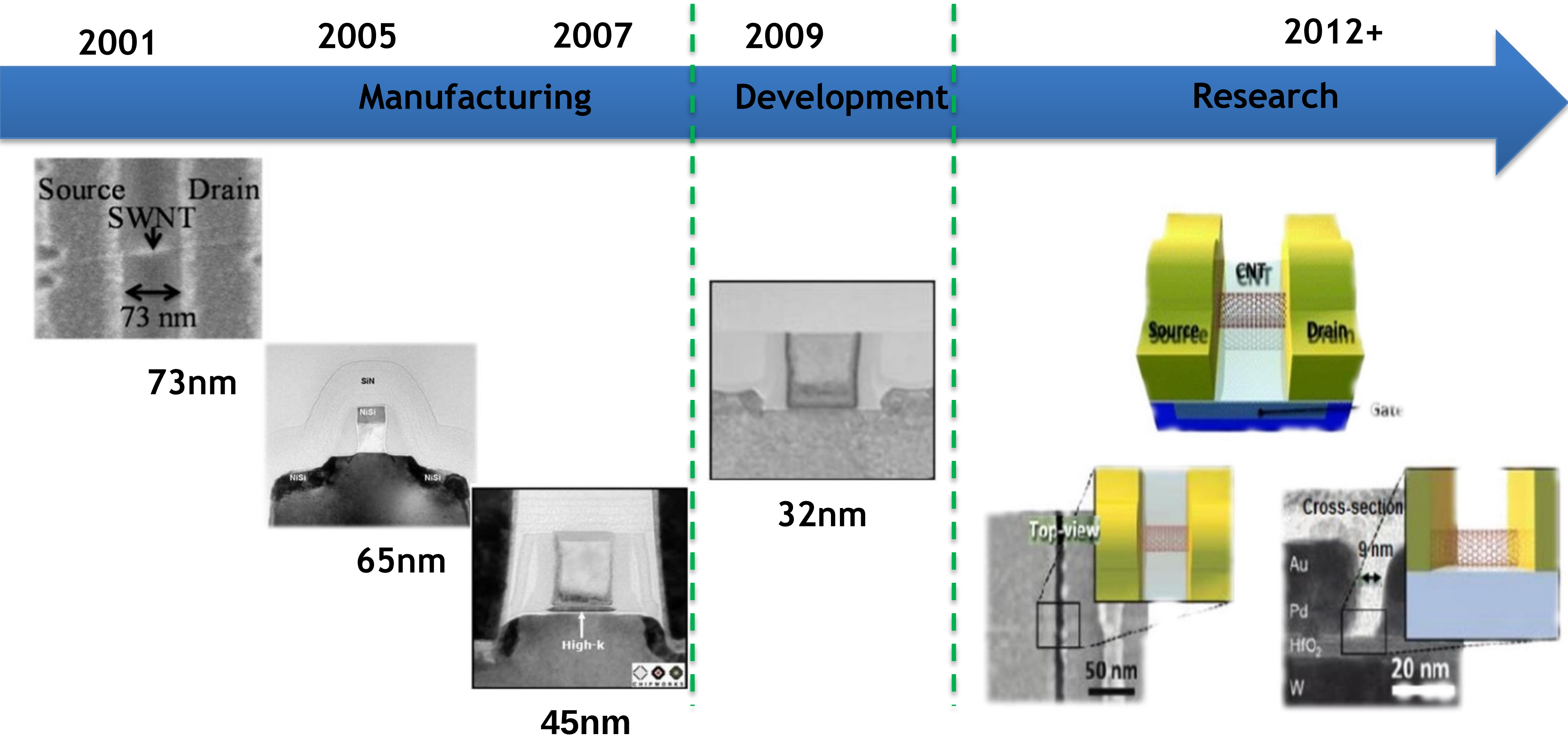


[Han et al. 2007]

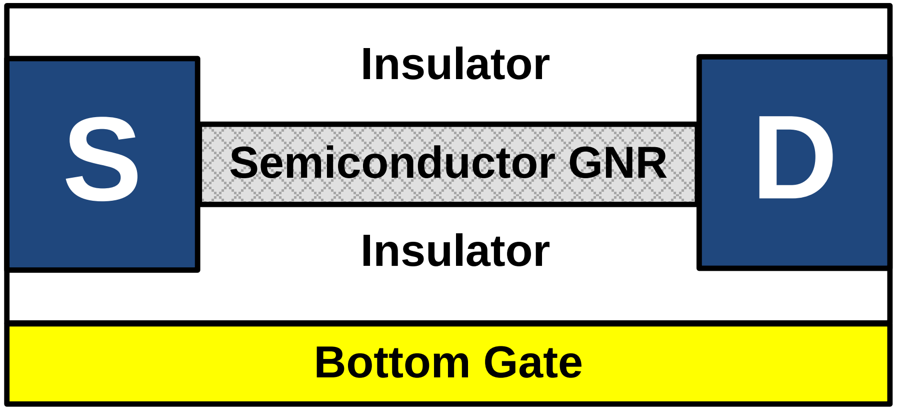
- Create band gap by confinement the graphene into graphene nanoribbon (GNR)[12]
- Li et al. **[12]** revealed that all sub 10nm pattern GNR is semiconducting with band gap proportional to its width

$$E_{gap} = \frac{0.8(eV \cdot nm)}{W(nm)}$$

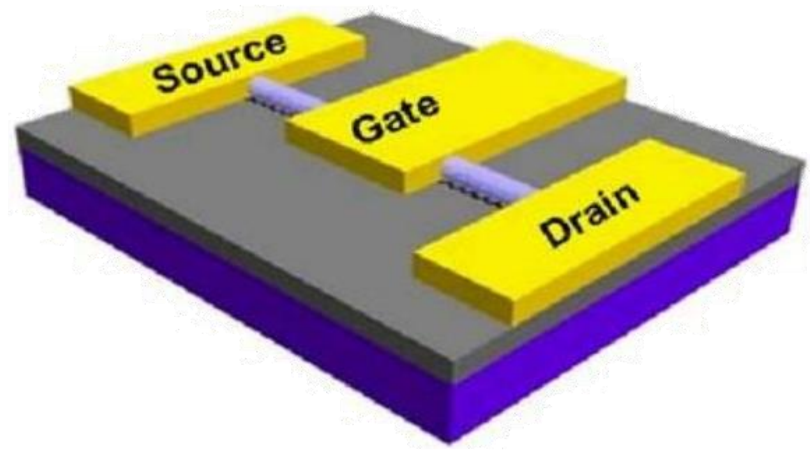
Transistor Research



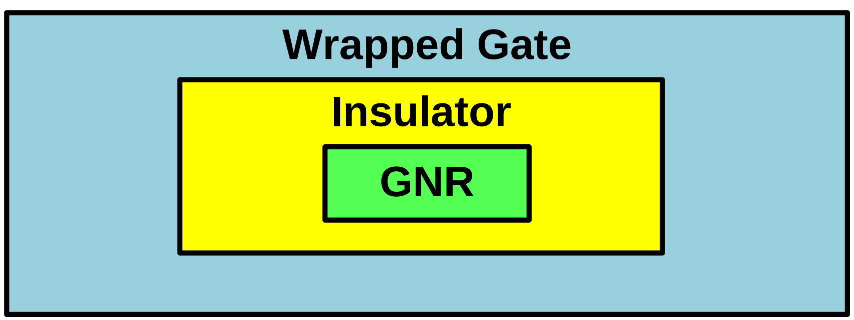
Device Structure of GNRFET



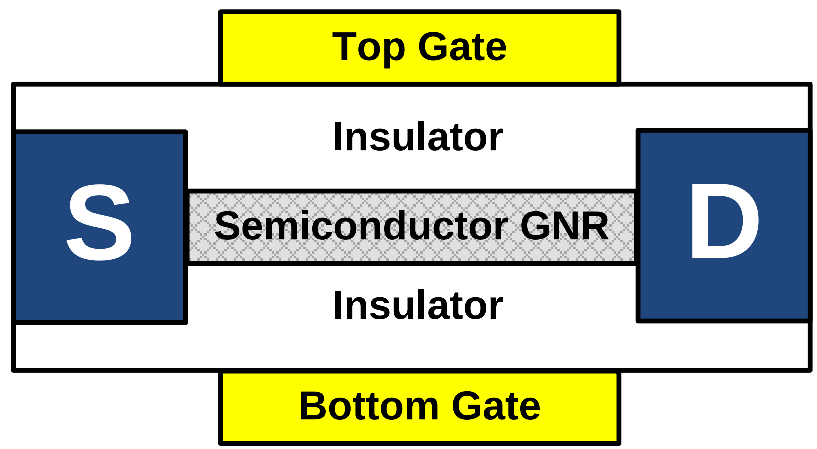
single gate
(Bottom gate electrode) GNRFET



Single gate
(Top gate electrode) GNRFET



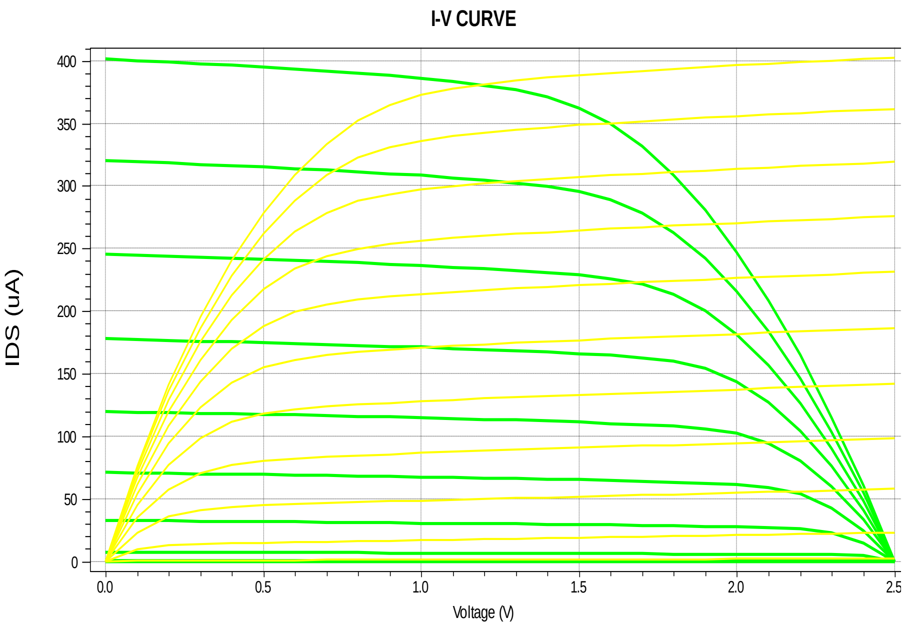
Wrapped Gate GNRFET
(in the plane normal to the channel direction)



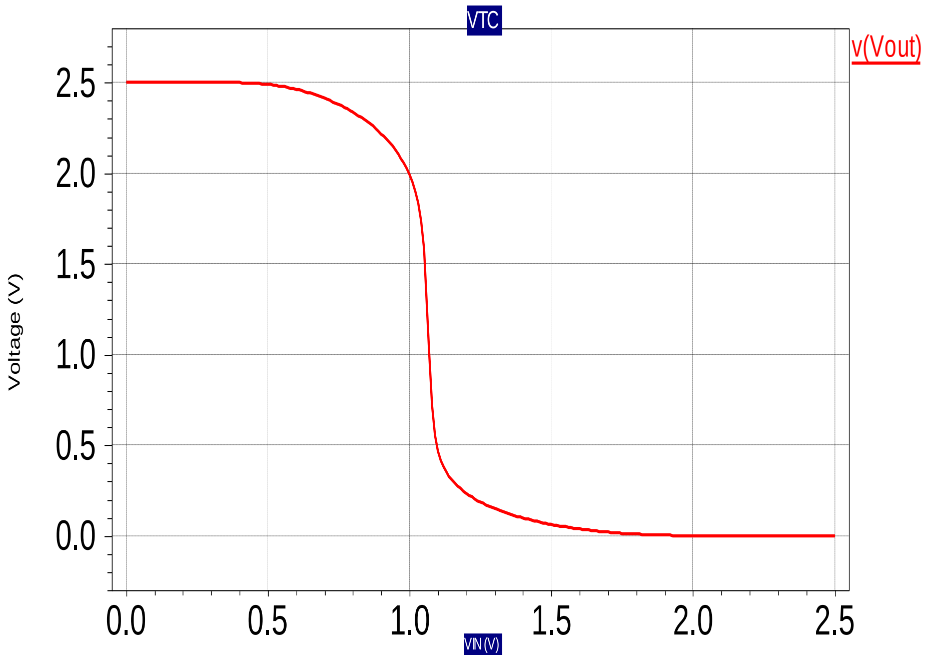
(GNR) FET
Double gate graphene nanoribbon

EXPERIMENT RESULT(SiCMOS)

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

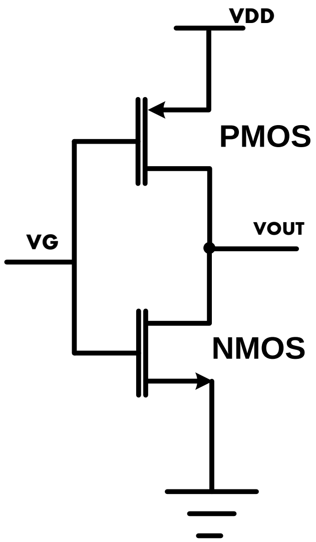


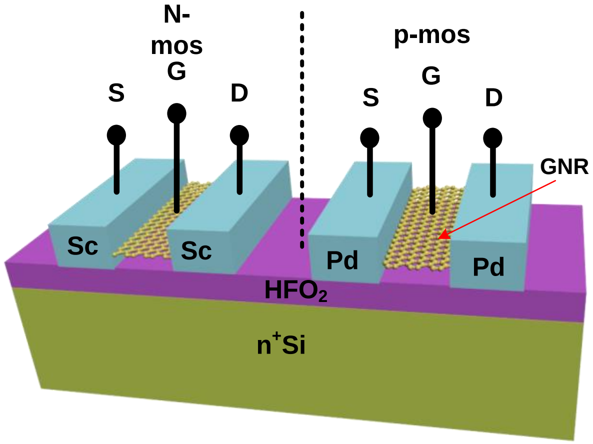
I-V Curve



VTC

MODELING(GNRCMOS)

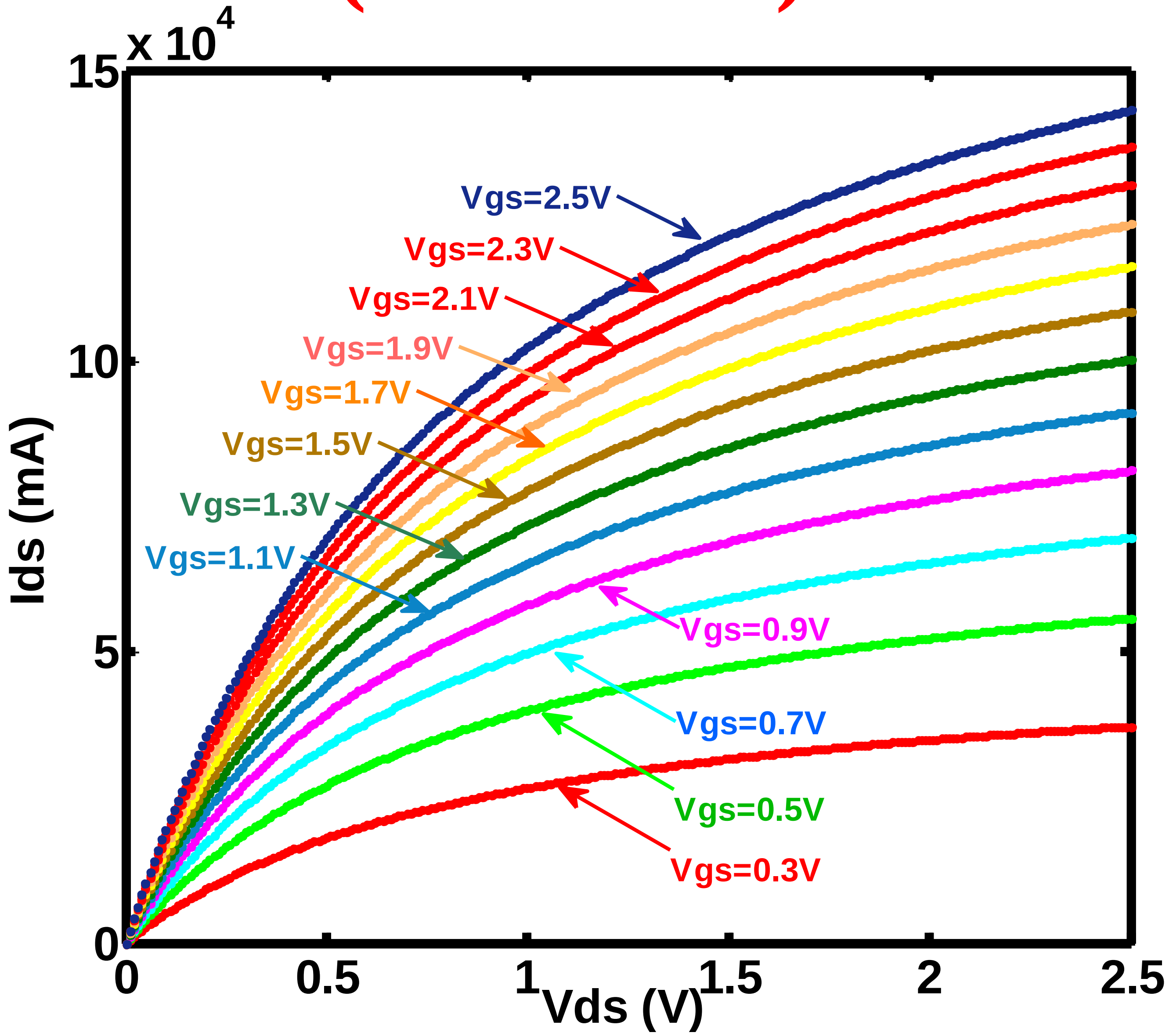




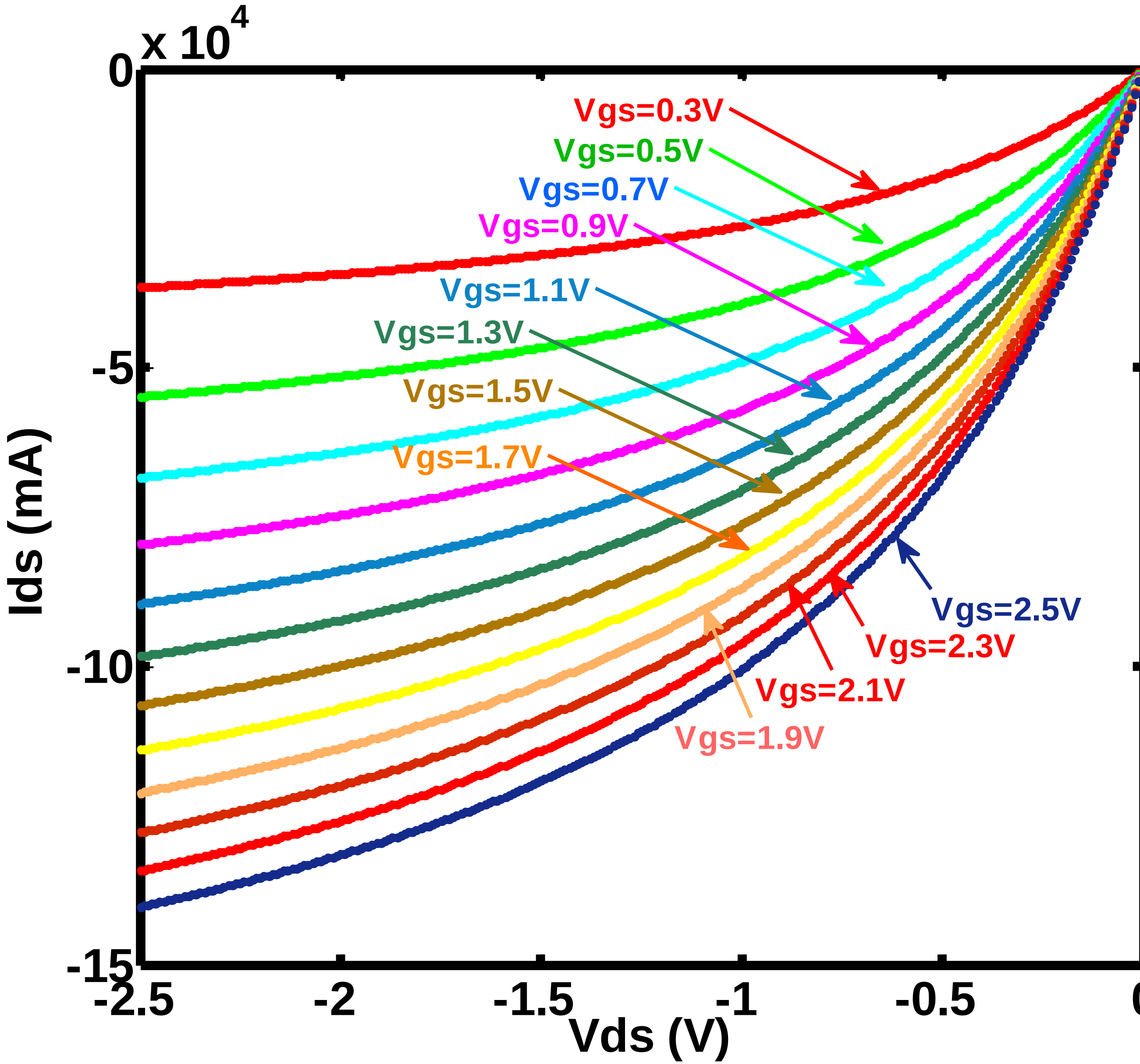
Hafnium-based oxides (HFO_2)are currently leading candidates to replace silicon oxide as a gate insulator in FET and CMOS to control the leakage current high k material owing to HFO2 is constant K is 25

$$I_{DN} = I_{DP}$$

NMOS-GNR (*I*-*V* Curve) for different V_{gs}

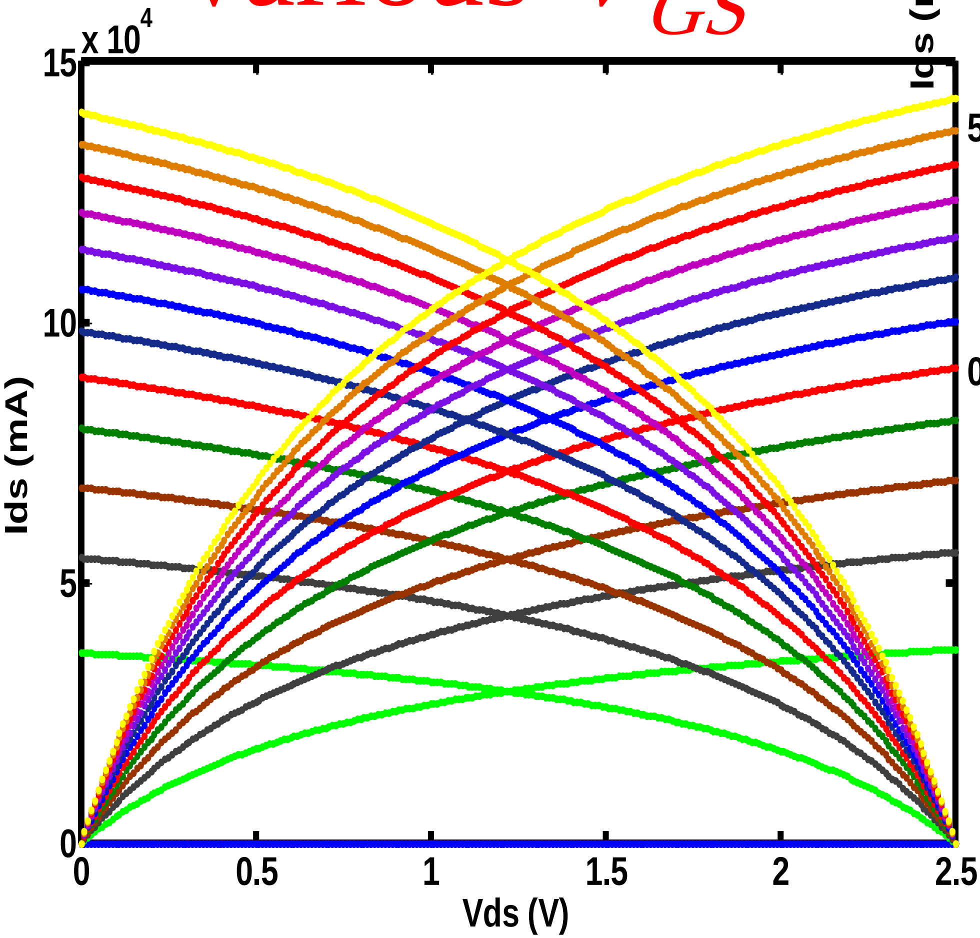


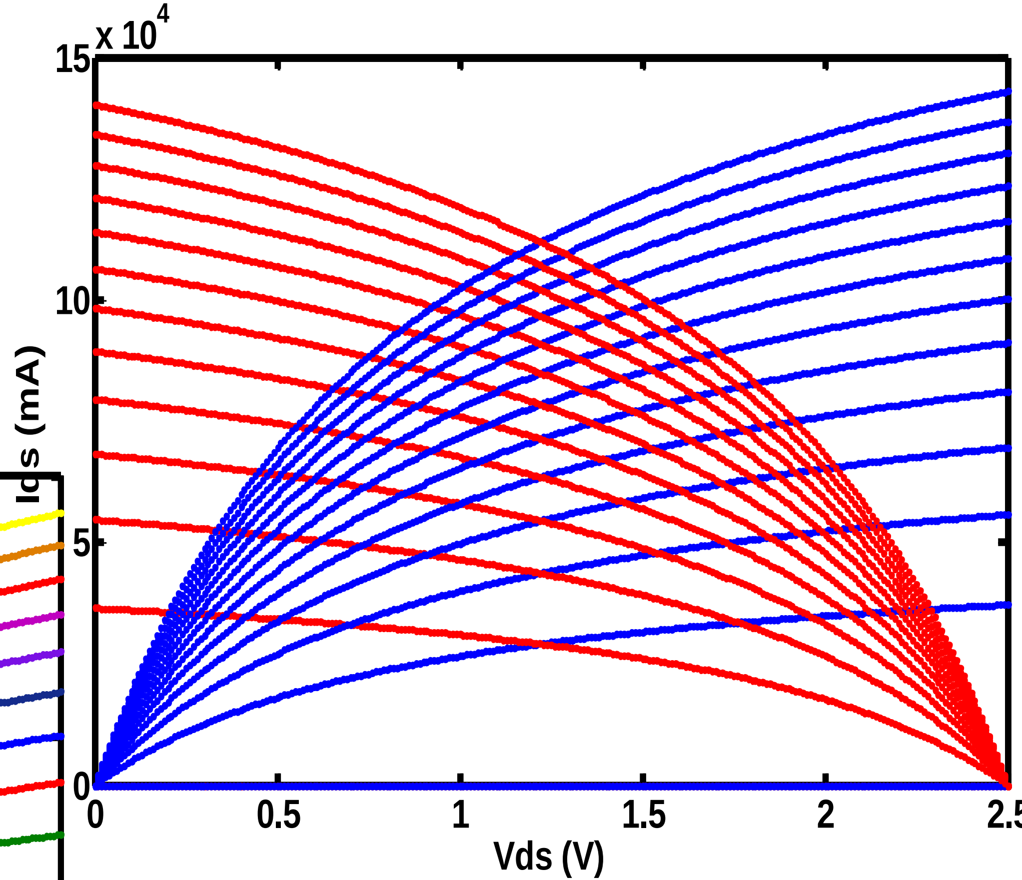
PMOS-GNR (*I*-*V* Curve) for different V_{GS}



I-V CURVE

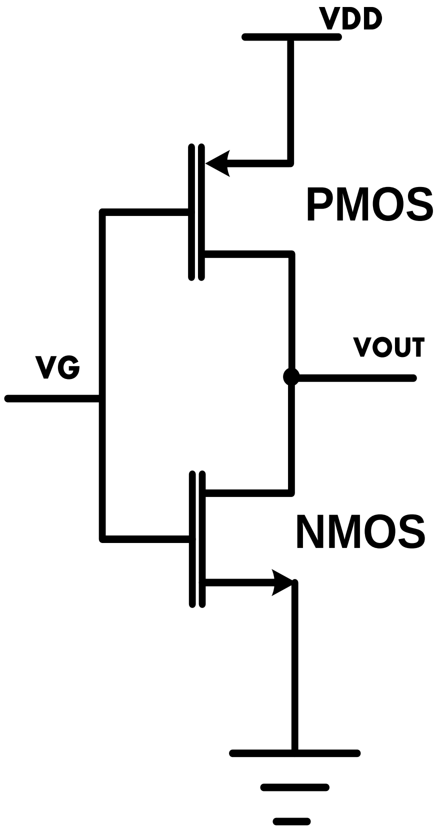
Differentiate Various V_{GS}

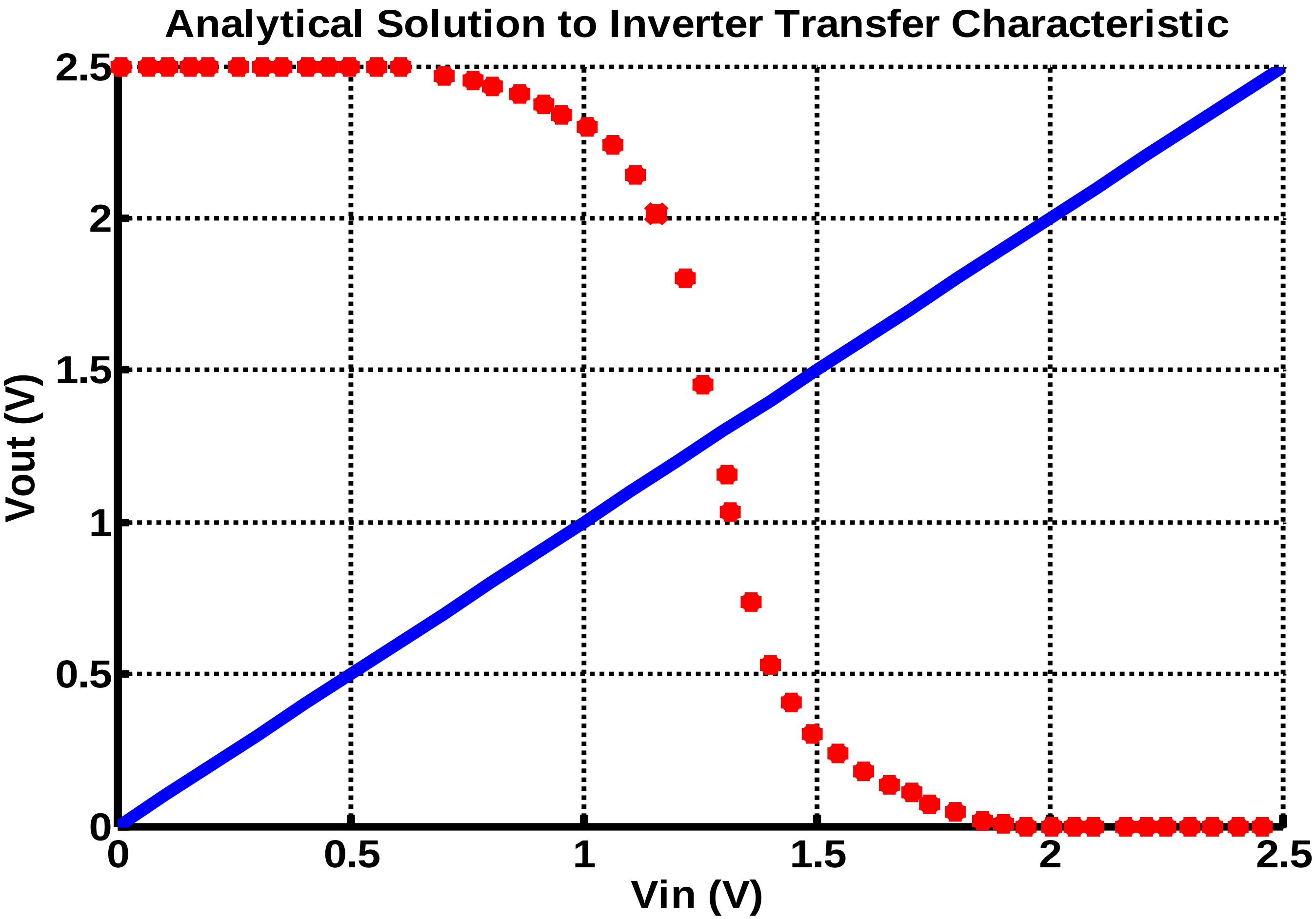




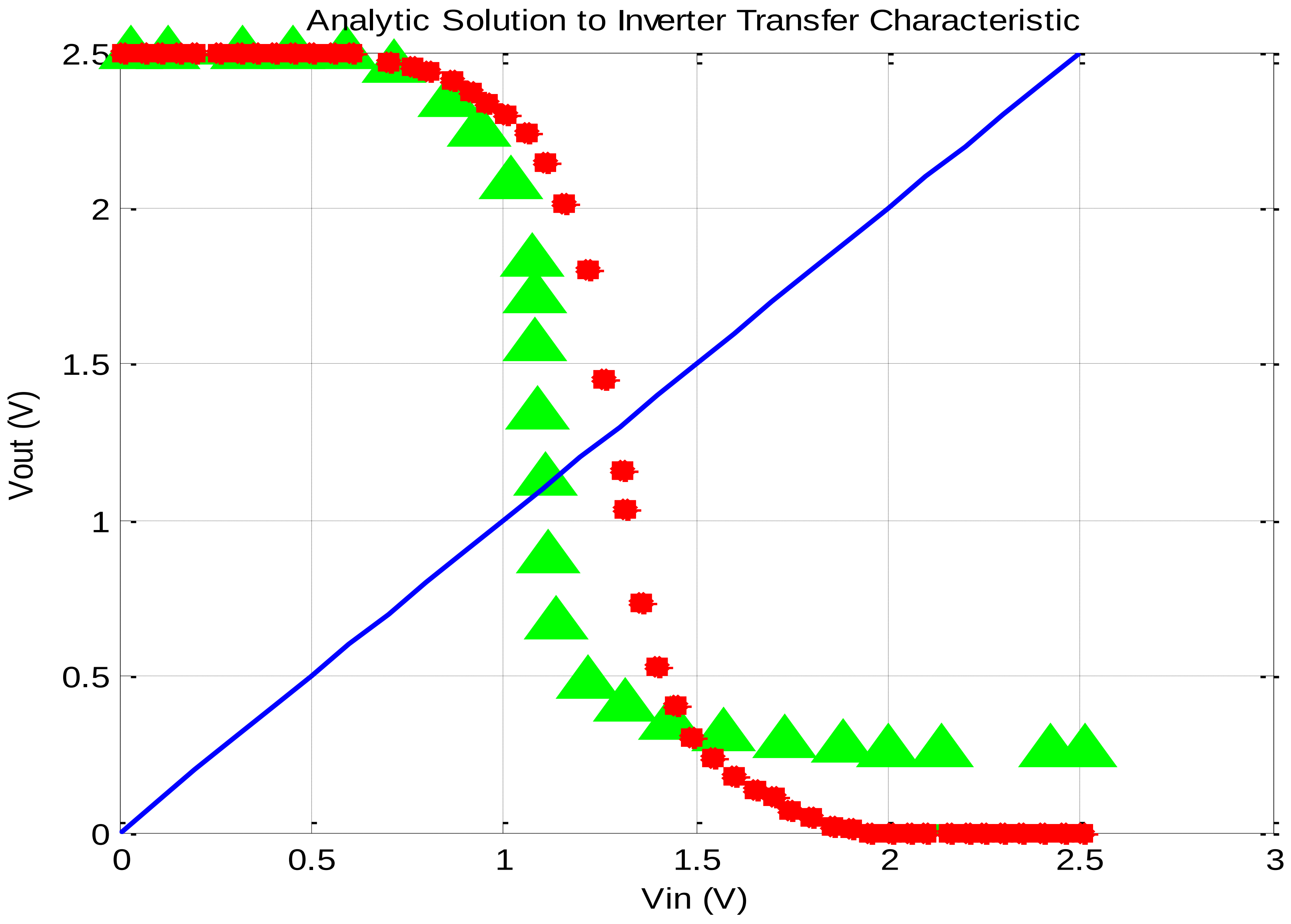
NMOS (Blue)
PMOS (Red)

VTC-GNR


VDD
PMOS
VG
VOUT
NMOS


Analytical Solution to Inverter Transfer Characteristic
Vout (V)
Vin (V)
0
0.5
1
1.5
2
2.5

COMPARISON RESULT



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شكرا جزيلا لإصغائكم

THANK YOU FOR YOUR LISTENING

Thank you

QUESTIONS?